Brahin Uddin

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Education

Rutgers University–New Brunswick Expected May 2028
B.S. Electrical Engineering, Minor in Computer Science *New Brunswick, NJ*

- GPA: 3.6 – Dean's List, Honors College, Engineering Honors Academy
- Coursework: Computer Architecture, Digital Logic Design, Semiconductors for AI (band structure, doping and transport, neuromorphic devices), Electronic Devices, Linear Systems & Signals, PCB Design, Data Structures

Experience

Data Center Facility Operations Intern May 2026 – Aug 2026
Crusoe *San Francisco, CA*

- Built the asset map for a deployed modular data center: 716 electrical, mechanical, security and life-safety assets, each linked to the asset that feeds it, from substation to rack PDU
- Found that maintenance records, SCADA tags and cloud dashboards named the same equipment differently; proposed a five-level naming standard, measured the live SCADA tags against it, and presented it to both team directors
- Wrote a Python parser that flattens nested SCADA/MQTT telemetry tag exports into CSV datasets, cutting on-site processing from hours to minutes (23 unit tests)
- Wrote a commissioning scope-of-work RFP for two new GPU data center buildings and a validation matrix that found 12 equipment types missing from the equipment lists

Low Voltage Systems Engineer Sep 2024 – Present
Rutgers Solar Car *Piscataway, NJ*

- Designed the "LV3 Core" mixed-signal carrier PCB (STM32G4) for battery telemetry and protection, with reverse-polarity protection, voltage sensing and buck regulation, and brought it up on the car
- Engineered a daisy-chained FDCAN network linking 8 distributed boards for real-time data between the high- and low-voltage managers and peripheral modules

Projects

Low-Latency Ethernet Market-Data Decoder Jul 2026 – Present
SystemVerilog, cocotb, Python, Vivado – Xilinx Zynq-7020 *brahinuddin.com/#u1*

- Designed a cut-through Nasdaq ITCH 5.0 decoder in SystemVerilog: Ethernet MAC, IPv4/UDP and MoldUDP64 parsers that decode fields while the frame is still arriving and roll back on a bad checksum; 73.5 ns median wire-to-record latency in simulation
- Designed a Gray-coded async FIFO to cross from the 125 MHz PHY clock to the 200 MHz core, and verified the full path against a Python golden model in a cocotb regression with fault injection, with zero mismatches
- Debugged the first Vivado implementation from 445 failing paths to timing closure at 200 MHz: moved the RGMII receive clock onto BUFIO/BUFR, tuned IDELAYE2 taps to center the data eye, and fixed CDC constraints broken by synthesis

RV32IM Five-Stage Pipelined RISC-V Core Mar 2026 – Jul 2026
SystemVerilog, Verilator, cocotb, Spike *brahinuddin.com/#u2*

- Designed an in-order RV32IM + Zicsr pipeline in SystemVerilog with full operand forwarding, a load-use interlock, precise exceptions and a pipelined multiply/divide unit
- Built the verification flow: cocotb unit tests per block, the riscv-tests and RISCOF suites (48/48, 47/47), and a lockstep harness comparing every retired instruction against Spike on random programs (12.5M instructions, zero divergences)
- Wrote the bare-metal startup code, linker script and console to run CoreMark, then broke down CPI with performance counters

NanoGuard: FPGA Pre-Trade Risk Gateway Oct 2026
Rutgers TechStart 2026, Top 5 Finalist – Verilog, Python, LLM API *brahinuddin.com/#u3*

- Conceived and prototyped an FPGA risk gateway for broker-dealers (SEC Rule 15c3-5); wrote the Verilog check pipeline (restricted list, size limit, price collar, capital limit) with every limit in a config register
- Built a Python flow where an LLM maps a plain-English rule onto a pre-verified hardware template that is validated, compiled to register values and human-approved; verified the RTL against a reference model on 100,000 random orders, zero mismatches

Technical Skills

- **RTL & FPGA:** Digital Design, Verification, Synthesis, Timing Closure, CDC; Verilog, SystemVerilog, Vivado, cocotb
- **Programming & Interfaces:** Python, Tcl, RISC-V Assembly, MATLAB, Java, Linux, Git/GitHub; UART, I2C, FDCAN
- **PCB & Lab:** KiCad, LTSpice, Mixed-Signal Design, Autodesk Fusion, Oscilloscopes, Soldering, 3D Printing
- **Familiar:** UVM, C, C++, SQL, ROS 2, Verilator, Yosys, ILA Debug, Ethernet MAC (RGMII/GMII, FCS/CRC-32), UDP/IPv4, MoldUDP64, AXI4-Lite